Background

Crest Factor Reduction (CFR) enhances the power efficiency of modern Radio Frequency Power Amplifiers (RFPA) when transmitting today's linear modulation schemes such as those utilised by 3G and 4G cellular systems. Systems4Silicon's FlexCFR technology is applicable to all modulation schemes including multi-carrier transmissions.

Prior to third generation (3G) cellular systems, wireless signals were relatively benign in that their envelope[1] was essentially constant. Subsequently (3G and beyond), the drive for enhanced data capacity has resulted in the wireless signal envelope becoming increasingly variable with the ratio between the signal peak and average power known as the Peak-to-Average-Power-Ratio (PAPR). The problem then is that the RFPA must be designed to enable transmission of the peaks of the signal power whilst, on average transmitting somewhat less power than this. Thereby, increasing PAPR leads to decreasing RFPA power efficiency and increased costs. By reducing the PAPR, CFR technology reduces these losses and saves the operator both capex and opex.

CFR typically functions by trading the signal's in-channel fidelity (e.g. EVM) for reduced PAPR whilst controlling out-of-channel spectral emissions. Systems4Silicon's FlexCFR is agnostic to the signal modulation and can operate in single or multi-channel modes. The operating configuration may be managed dynamically, thereby adapting for varying signal composition such as may be encountered in Distributed Antennas Systems (DAS). Operating bandwidth is only limited by the capabilities of the underlying hardware meaning that today's high-end FPGA's can support FlexCFR for composite signals upwards of 150 MHz.

Systems4Silicon has supplied its CFR and associated Digital PreDistortion (DPD) technology to an international customer base since 2008. The IP is delivered and supported by engineers with deep experience of wireless transmitter development, thereby optimising successful integration.

[1] The variation of the instantaneous size of the signal as it is modulated with the digital data.

Applications

Crest Factor Reduction for single or multi-carrier (mixed-mode) power amplifiers transmitting signals such as 4G, 3G, DVB-T, DVB-S2X, BGAN, APCO P25 etc. operating in either TDD or FDD mode. The FlexCFR IP is not pre-configured for the transmission standard, therefore it will also operate with legacy and bespoke transmission technologies – please contact Systems4Silicon to discuss your specific requirements.

Figure 1 illustrates one example of how Systems4Silicon's FlexCFR may be integrated within a typical sub-system. The use of a DPD block following the CFR function is not mandated, however if it is required then Systems4Silicon can supply its DPD Toolkit IP.

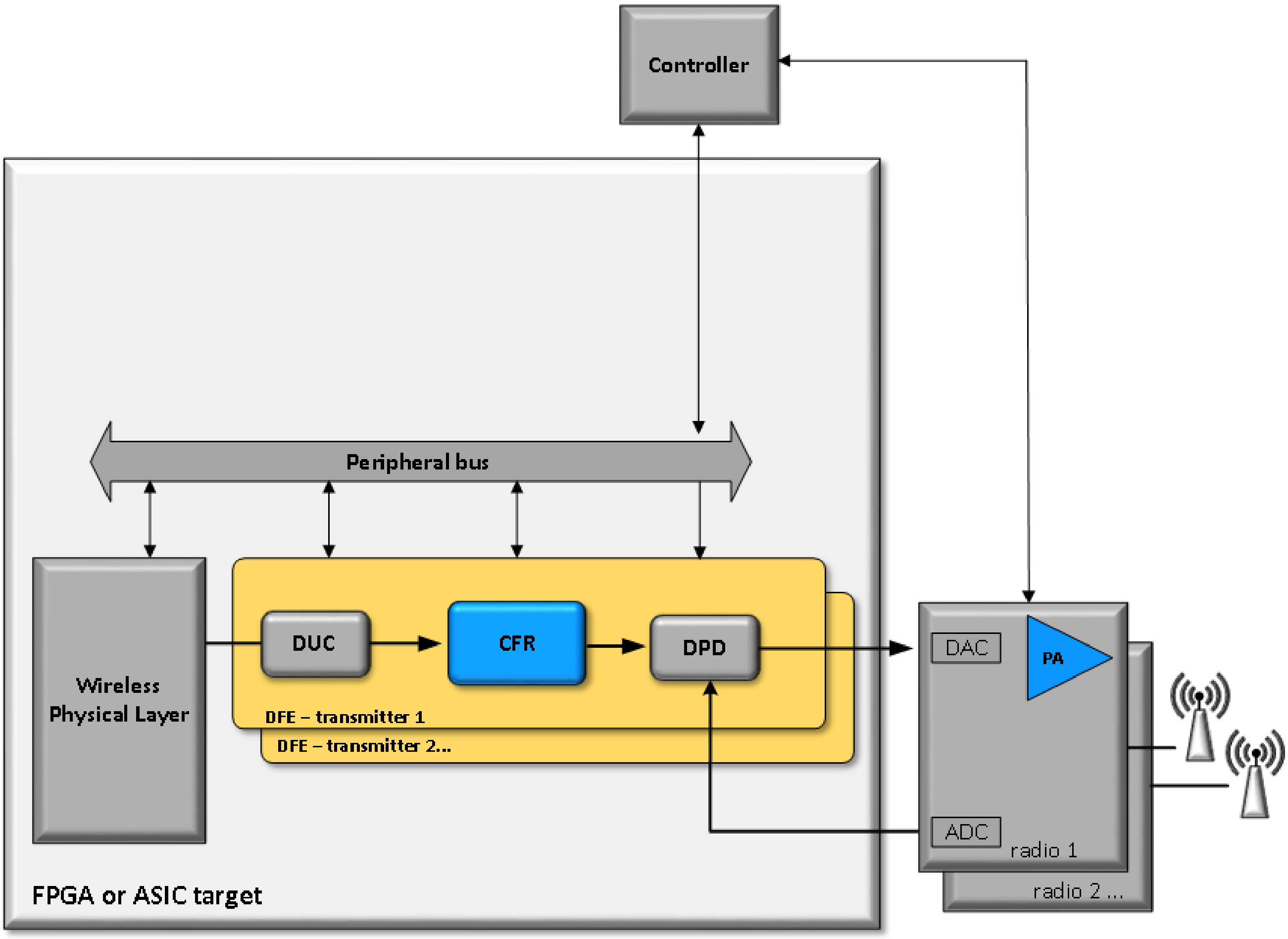

Figure 1: FlexCFR example sub-system architecture.

Systems4Silicon's FlexCFR is implemented in RTL as an IP Core which is targeted at the real-time hardware (FPGA/ASIC). Software configuration and control is a lightweight, non-real-time function provided by the host system's Controller.

Performance

Table 1 illustrates the performance of the FlexCFR operating in a 20 MHz band occupied by LTE (4G) signals.

Table 1: FlexCFR example 4G performance (64-QAM carriers within a 20 MHz band).

LTE Carrier Configuration	Output PAPR at 0.01% (dB)	ACLR (dB)	EVM (%)
5 MHz	7.3	> 52	5.0
10 MHz	7.0	> 52	5.0
15 MHz	7.0	> 52	5.0
20 MHz	7.0	> 52	5.0
2 x 10 MHz	7.1	> 52	5.0

Figure 2 illustrates the Complementary Cumulative Distribution Function (CCDF) before and after the application of FlexCFR at the RFPA output for a single carrier 10 MHz LTE signal.

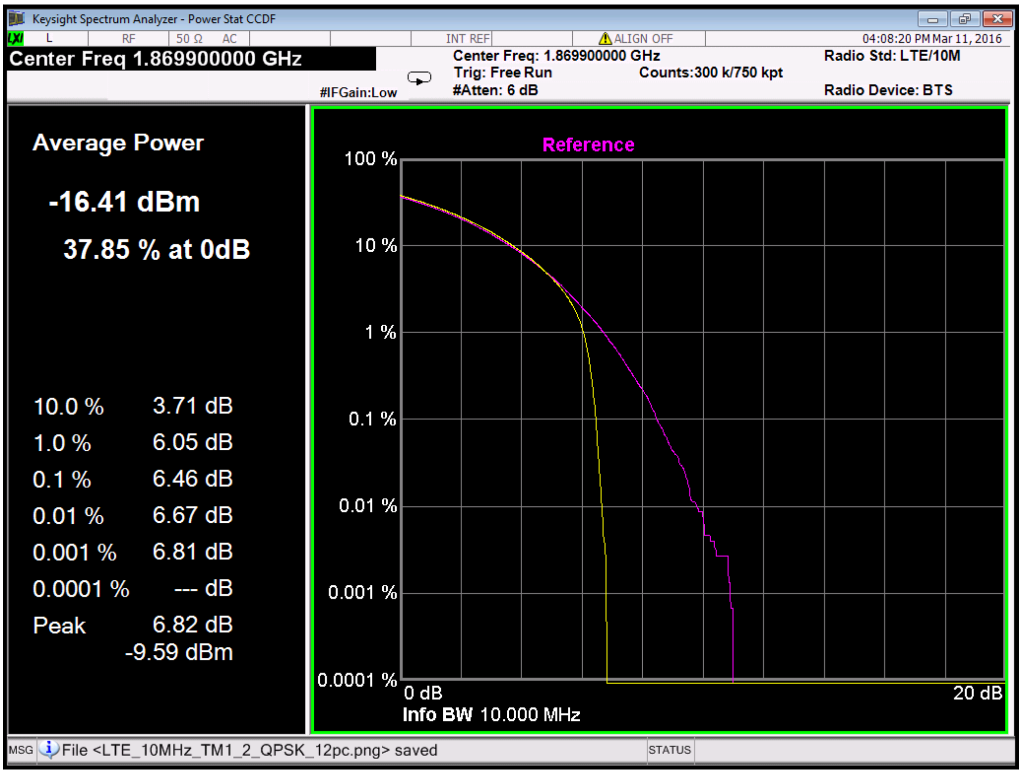

Figure 2: CCDF for 10 MHz LTE, TM1.2 with 12% EVM.

Features & Capabilities

Feature	Comment
PAPR reduction capability	Single or multi-carrier signals with static or dynamically varying composition and average power level.
Latency	Low latency afforded by a high-performance, single-iteration architecture.
Supported transmission bandwidth	Limited only by the capabilities of the FPGA/ASIC (i.e. the attainable system clock rate). State of the art with today’s FPGA devices is approximately 150 MHz of modulation bandwidth.
Supported Tx channels	Unlimited. One FlexCFR instance is required per antenna.
PA technology	Agnostic with respect to PA transistor technology or PA topology (e.g. GaS, GaN, LDMOS, Doherty, Class A/B, Envelope Tracking, …)
Transmission standards	Agnostic with respect to transmission standard (e.g. 3G, 4G, DVB, APCO P25, BGAN and many others) and air access technique (e.g. FDD/TDD), including multi-carrier and mixed mode operation.
RFPA efficiency improvement	This is not a valid metric for any CFR system. The maximum, post-CFR PAPR should first be established and then RFPA designed with this in mind. Generally speaking, the lower the achieved PAPR, the higher the resulting RFPA efficiency.
Convenience	In-deployment algorithmic training or calibration is not required, either at power-up or subsequently.
Digital PreDistortion (DPD)	DPD and CFR are different yet complimentary technologies that both facilitate the enhancement of PA efficiency. Although often used together for optimum efficiency, this is a system design decision and not mandatory. Systems4Silicon’s CFR operates with or without a following DPD function.

Target Device Resources

The implementation of FlexCFR is compact. Table 2 illustrates the resource utilisation for a typical single antenna implementation on Microsemi PolarFire. Table 3 illustrates the resource utilisation of the same design on Microsemi SmartFusion2. Note that these figures are for guidance only and may vary with factors such as the specific tools settings, total device utilisation etc.

Table 2: FlexCFR resource utilisation for Microsemi PolarFire part number MPF300T

	4LUT	DFFs	1k uSRAM	20k LSRAM	18x18 MACC
FlexCFR	5,169	7,296	4	1	28
Device Total	**299,544**	**299,544**	**2,772**	**952**	**924**
Utilisation	**1.73%**	**2.44%**	**0.14%**	**0.11%**	**3.03%**

Table 3: FlexCFR resource utilisation for Microsemi SmartFusion2 part number M2S025

	4LUT	DFFs	1k uSRAM	18k LSRAM	18x18 MACC
FlexCFR	5,331	7,158	4	1	28
Device Total	**27,696**	**27,696**	**34**	**31**	**34**
Utilisation	**19.25%**	**25.84%**	**2.94%**	**3.23%**	**82.35%**

Availability

Systems4Silicon's FlexCFR IP is immediately available for FPGA and ASIC targets together with a comprehensive Engineering Data Sheet plus integration facilities. To discuss your specific implementation requirements please contact Systems4Silicon (details below).

Contact

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