FlexDPD: Overview

Background

Digital Predistortion technology (DPD) enables power-efficient transmission in modern wireless communications systems.

Prior to the 3G cellular system, wireless signals were relatively benign in that their envelope (i.e. the variation of instantaneous RF signal magnitude as it is modulated with the digital data) was essentially constant. Subsequently, (3G and beyond) the drive for enhanced data capacity has resulted in the wireless signal envelope becoming increasingly dynamic. This poses significant challenges for the transmitter and in-particular the power amplifier (PA). Efficient power amplifiers tend to be non-linear, which is fine when the signal envelope is benign, however non-linear transmission of 3, 4 and 5G signals result in the generation of interference, which can exceed regulatory requirements. To fix this there are essentially two options, but only one practical choice:

- Design a linear PA; such designs are expensive and highly inefficient. For example, to transmit 20 Watts the PA would probably consume ~400 Watts or more, hence around 5% efficiency. **OR …**

- Linearize the PA by dynamic manipulation of the PA itself and/or its input signal. DPD is a linearization technology which enables interference-free transmission using an essentially non-linear (i.e. power efficient) PA. Efficiencies in excess of 50% are attainable, thereby facilitating significant savings in terms of power supply capacity and thermal design before even considering the operational saving of over 350 Watts for the above example.

Since 2008, drawing on over thirty years of radio transmitter product design expertise, Systems4Silicon has supplied, supported and evolved its FlexDPD technology to an international customer base. Development of algorithms for DPD is complex and time consuming with the resulting solution putting significant demands upon the underlying signal processing resources. Systems4Silicon's FlexDPD is readily scaled to optimise these demands according to the needs of the customer's system. It is unique to the marketplace since it is delivered as IP cores for any ASIC or FPGA. Therefore, since Systems4Silicon and the IP are independent of device vendor, this facilitates design migration between FPGA vendor devices, or from FPGA to ASIC and flexibility in the selection of the radio transceiver device.

Applications

The linearization of single-carrier, multi-carrier or mixed-mode transmissions for contemporary standards such as 3G/4G/5G and DVB operating in either TDD or FDD mode. Since FlexDPD is not specifically configured for the transmission standard it will also operate with legacy and bespoke transmission technologies – please contact Systems4Silicon to discuss your specific requirements.

Figure 1 illustrates one example of how Systems4Silicon's FlexDPD may be integrated within a typical sub-system.

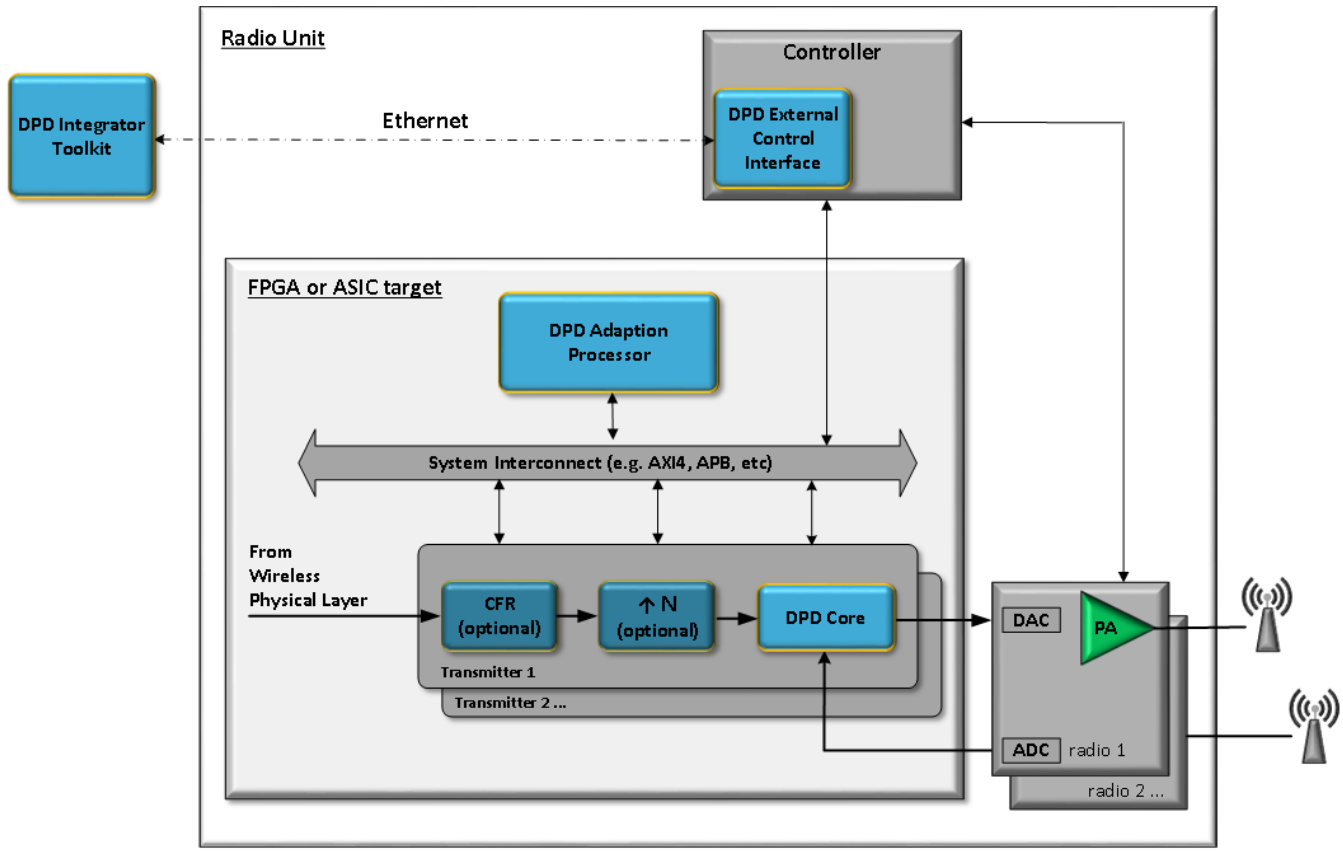

Figure 1: FlexDPD example sub-system architecture.

FlexDPD comprises a software adaption processing algorithm (the Adaption Processor) and a DPD Core which is targeted at the real-time hardware. The Adaption Processor is coded in portable C++ for targeting at (for example) an FPGA soft-core processor, ARM Cortex hard processor or other dedicated µP/DSP.

The DPD Core comprises the DPD predistortion engine, transmit and observation path data capture functions and optional linear distortion compensations for the analogue hardware.

The DPD Core is implemented to accommodate individual clock domains for transmit path, observation path and the control plane and has fully deterministic sample latency. The Adaption Processor requires access to memory for run-time data storage, however it is non-real-time and can share such resources with customer applications.

Typically, a hardware platform includes a Controller unit[1] for the configuration and control of platform peripherals such as data converters, analogue gain etc.; the same Controller would be used to manage the operation of FlexDPD. During operation, in addition to the linearization function the Adaption Processor determines other correction values required to optimise system performance, for example transmitter gain and analogue quadrature modulator (AQM) imperfection compensation. These low-rate signals are communicated to the Controller for application to the appropriate hardware actuators in the radio.

Performance

The screenshots in Figure 2 provide an illustration of the practical performance in relation to the improvement of unwanted spectral emissions. In both cases the PA is Doherty architecture with output power of +46 dBm. The left-hand trace is illustrative of a mixed-mode 4G plus multi-carrier 2G transmission (i.e. dissimilar Radio Access Technologies) with 45 MHz instantaneous bandwidth, whereas the other is multi-carrier LTE.

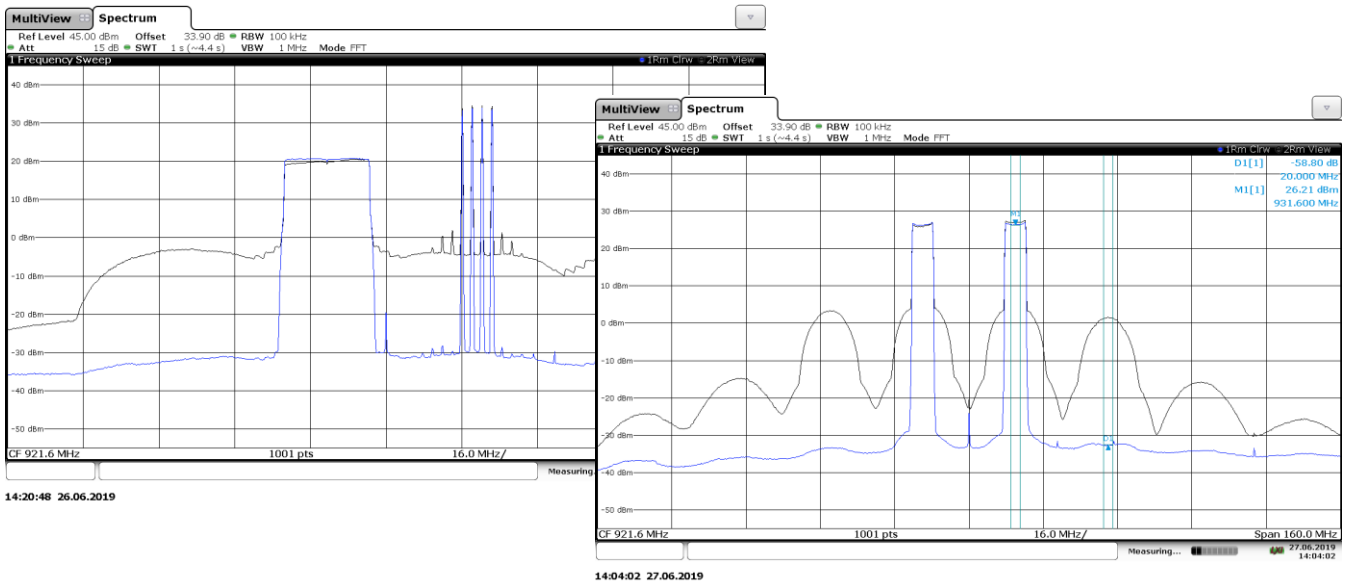

Figure 2: FlexDPD illustrative performance.

[1] Which could be another embedded processor.

Support

Systems4Silicon's FlexDPD is supplied with comprehensive engineering data sheets and our DPD Integrator support applications, which provide graphical performance and behavioural metrics for the linearized transmitter system (see Figure 3Figure 1). At the heart of this system is the Developer Assist data logging and presentation application, the file outputs of which may be reviewed locally by the system integrators or delivered to Systems4Silicon thereby facilitating remote support.

Furthermore, Systems4Silicon will not simply wave goodbye following IP delivery. The DPD component is just one technology in a linearized transmitter system and within such systems, regardless of the DPD supplier, both the radio and (more obviously) the PA itself impact on the overall attainable performance. For example, the PA should be designed with linearization in mind and the radio bandwidth must be suitable for the anticipated linearized performance. Such design decisions and trade-offs are facilitated partly by the scalability of the FlexDPD solution, however, no less important than this is the detailed engineering knowledge and dedicated support that is provided by the Systems4Silicon team to help you attain the optimum performance for your system. Without such support, a typical DPD IP "black box" would become difficult to manage and optimise. Systems4Silicon's IP plus the support facilities are designed to smooth the development process.

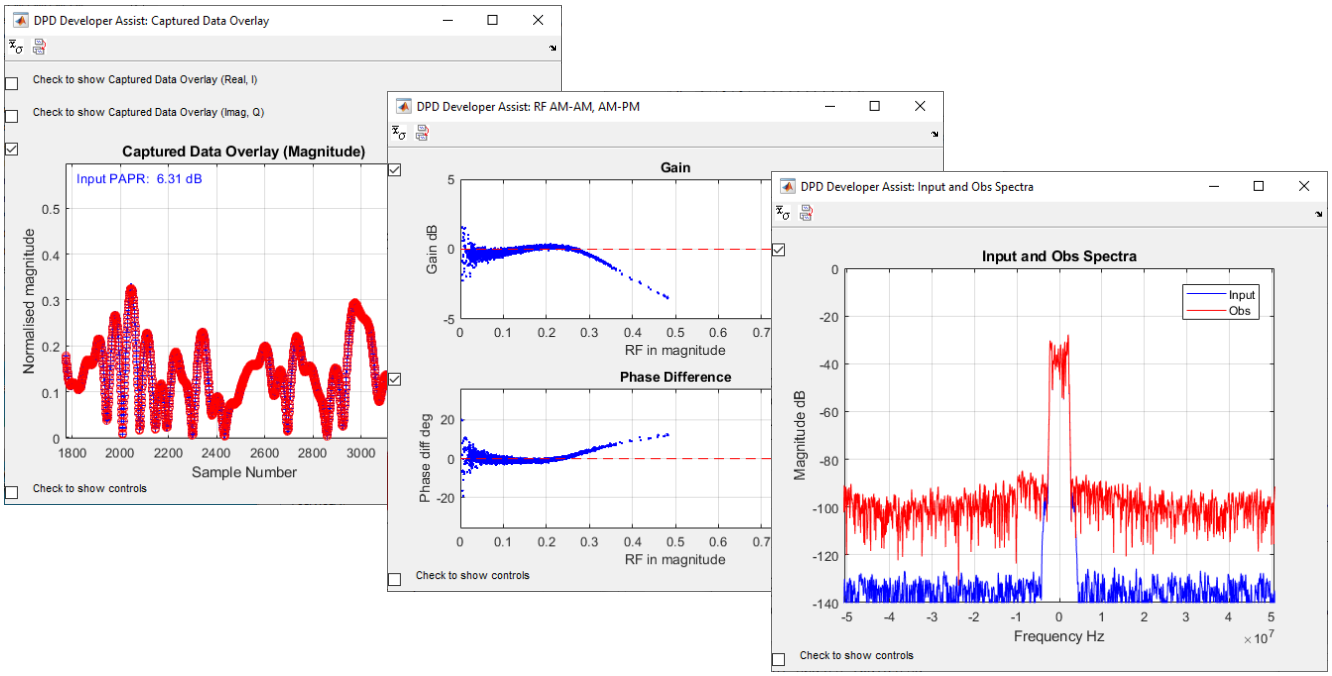

Figure 3: DPD Developer Assist integration support tool, example outputs.

Features & Capabilities

Feature	Comment
Correction capability (non-linear)	Up to 40 dB or better ACLR improvement depending upon the DPD configuration and system specifications/characteristics.
Correction capabilities (linear)	Adaptive AQM dc-offset and imbalance correction for either (or both) the transmit and observation path. Adaptive gain and phase slope correction. Adaptive gain control.
Supported Tx bandwidth	Limited only by the capabilities of the FPGA/ASIC and of the radio sub-system (e.g., the attainable system clock rate, available FPGA resources, analogue radio bandwidth etc.).
Supported Tx channels / MIMO	Limited only by the resources of the FPGA/ASIC and specification of the radio sub-system. Target technology system resources may be optimised by commutating the use of the FlexDPD's Data Acquisition sub-system and the Adaption Processor between multiple channels.
PA technology	Agnostic with respect to PA transistor technology or PA topology (e.g., GaS, GaN, LDMOS, Doherty, Class A/B, Envelope Tracking, …).
Transmission standards	Agnostic with respect to transmission standard (e.g., 2/3/4/5G, DVB-T, BGAN, DVB-S2X and many others) and air access technique (e.g., FDD/TDD), including multi-carrier and mixed mode (multi-RAT) operation.
DPD update cycle period	Typically, 100 ms for a single channel system (processor dependent). Rapid convergence algorithms result in system ACLR typically better than 1 dB of nominal minimum within 2-3 update cycles.
Memory correction	Scalable and dynamically configurable as demanded by the PA characteristics.
PA efficiency improvement	This is not a valid metric for any DPD implementation. Typically a PA will be designed to meet a particular efficiency and then the DPD enables linear behaviour at that efficiency. If, in order to meet spectral emissions, the drive to a particular PA has had to be reduced then the DPD will help to recover the original operating power level and hence efficiency. If the PA has been over-designed for the target operating power then the DPD may enable the output power and efficiency to be increased whilst maintaining linear transmission. Using the latest GaN transistors in a Doherty configuration, it is possible to attain efficiencies in the region of 50% or higher depending upon system characteristics.
Convenience	In-deployment algorithmic training or calibration is not required, either at power-up or subsequently.
Crest Factor Reduction (CFR)	Crest Factor Reduction (CFR) and DPD are different, yet complimentary, technologies that both facilitate the enhancement of PA efficiency. Although often used together for optimum efficiency, this is a system design decision and not mandatory. Systems4Silicon's FlexDPD operates with or without a preceding CFR function.

Target Device Resources

In addition to FlexDPD being scalable according to the application, the implementation is extremely compact. Table 1 illustrates the resource utilisation for a typical implementation on Xilinx Zynq 7000 of a single channel system that includes comprehensive memory correction capabilities necessary for broadband operation. For this target device the embedded Arm core can be utilised for the DPD adaption processing and the demands upon the device fabric are very small indeed.

Table 1: FlexDPD resource utilisation for Xilinx Zynq 7000 part number XC7Z045

	LUTs	Registers	DSPs	Block Memory Kbits
DPD Core	6,473	6,471	110	738
Utilisation	**< 3.0%**	**< 1.5%**	**< 12.2%**	**< 3.8%**

Availability

Systems4Silicon's FlexDPD IP is available now for FPGA and ASIC targets together with data sheets and DPD Integrator support tools. To discuss your specific implementation requirements please contact Systems4Silicon using any of the channels below.

Contact

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