Background

Digital Predistortion technology (DPD) enables power-efficient transmission in modern wireless communications systems. Prior to third generation (3G) cellular systems, wireless signals were relatively benign in that their envelope (i.e. how the instantaneous size of the signal varies as it is modulated with the digital data) was essentially constant. Subsequently (3G and beyond) the drive for enhanced data capacity has resulted in the wireless signal envelope becoming increasingly noise-like. This poses significant challenges for the transmitter and in-particular the power amplifier (PA). Efficient power amplifiers tend to be non-linear, which is fine when the signal envelope is benign, however the non-linear transmission of 3, 4 and 5G signals result in the generation of troublesome interference, which can exceed regulatory requirements. To fix this there are essentially two options, but only one practical choice:

- Design a linear PA; such designs are expensive and highly inefficient (e.g. to transmit 20 Watts the PA would probably consume ~400 Watts or more). Or

- Linearize the PA by a dynamic manipulation of the PA itself and/or its input signal. DPD is a linearization technology which enables interference-free transmission using an essentially non-linear (i.e. power efficient) PA.

Since 2008, drawing on over thirty years of transmitter product design expertise, Systems4Silicon has supplied, supported and evolved its FlexDPD technology to an international customer base. Development of algorithms for DPD is complex, costly and time consuming and the resulting solution may put significant demands upon the underlying signal processing resources. Systems4Silicon's FlexDPD is readily scaled to optimise these demands according to the needs of the customer's system. It is unique to the marketplace since it is delivered as IP cores for any ASIC or FPGA and since Systems4Silicon is independent of a device vendor this facilitates design migration between FPGA vendors' devices and from FPGA to ASIC.

Applications

The linearization of single or multi-carrier (mixed-mode) power amplifiers for contemporary transmission standards such as LTE, WCDMA and DVB operating in either TDD or FDD mode. Since the DPD IP is not specifically configured for the transmission standard it will also operate with legacy and bespoke transmission technologies – please contact Systems4Silicon to discuss your specific requirements.

Figure 1 illustrates one example of how Systems4Silicon's FlexDPD may be integrated within a typical sub-system.

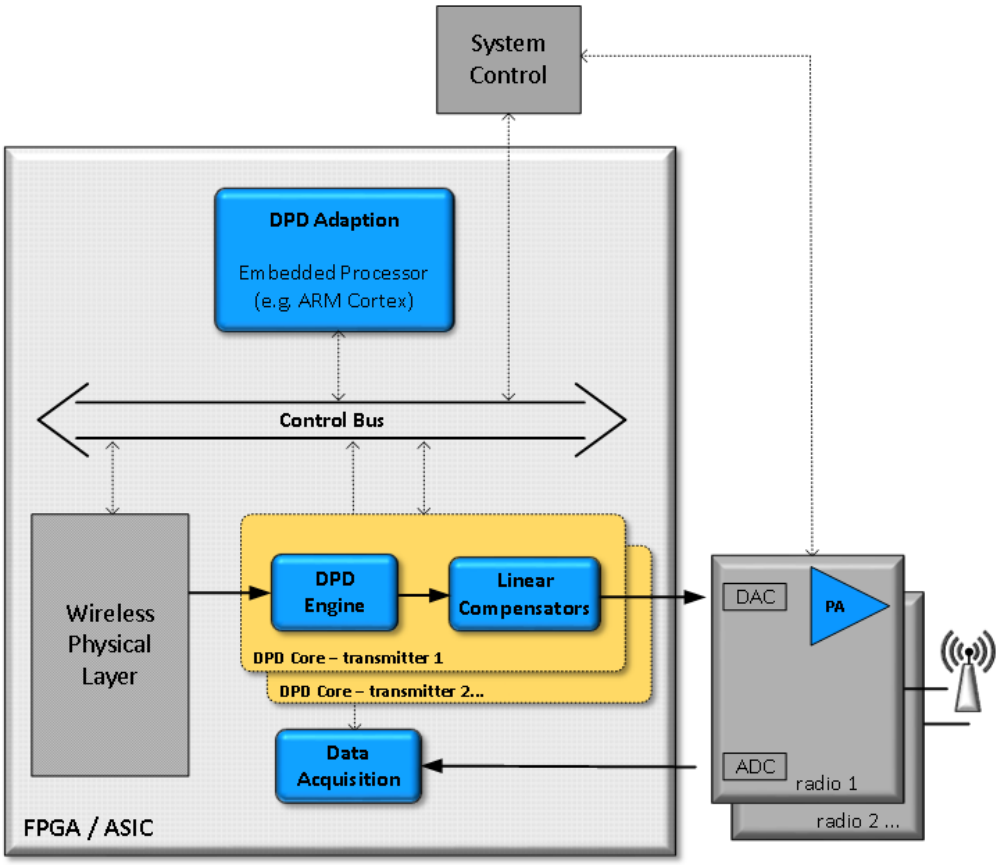

Figure 1: FlexDPD example sub-system architecture.

FlexDPD comprises a software adaption processing algorithm (the Adaption Processor) and a DPD Core which is targeted at the real-time hardware. The Adaption Processor is coded in portable C++ for targeting at (for example) an FPGA soft-core processor, ARM Cortex hard processor or other dedicated µP/DSP.

The DPD Core comprises the DPD Engine, transmit and observation path data capture functions and linear distortion compensation for the analogue hardware. For platforms with analogue hardware that introduces low levels of linear distortion the compensation function can be omitted to minimise total resource requirements.

The DPD Core is implemented to accommodate individual clock domains for transmit path, observation path and the control plane and has fully deterministic sample latency. The Adaption Processor requires access to memory for run-time data storage, however it can share such resources with customer applications.

Typically, a hardware platform includes a Controller unit[1] for the configuration and control of platform peripherals such as data converters, analogue gain etc.; the same Controller would be used to manage the operation of the DPD. During operation, in addition to the linearization function the Adaption Processor determines other correction values required to optimise system performance, for example transmitter gain and analogue quadrature modulator (AQM) imperfection compensation. These low-rate signals are communicated to the Controller for application to the appropriate hardware actuator in the radio.

Performance

The screenshots in Figure 2 provide an illustration of the practical performance in relation to the improvement of unwanted spectral emissions. In both cases the PA is Doherty architecture and the waveforms exhibit a peak to average power ratio of ~10 dB. The left-had trace is illustrative of a mixed-mode UMTS and LTE transmission, whereas the other is single carrier LTE.

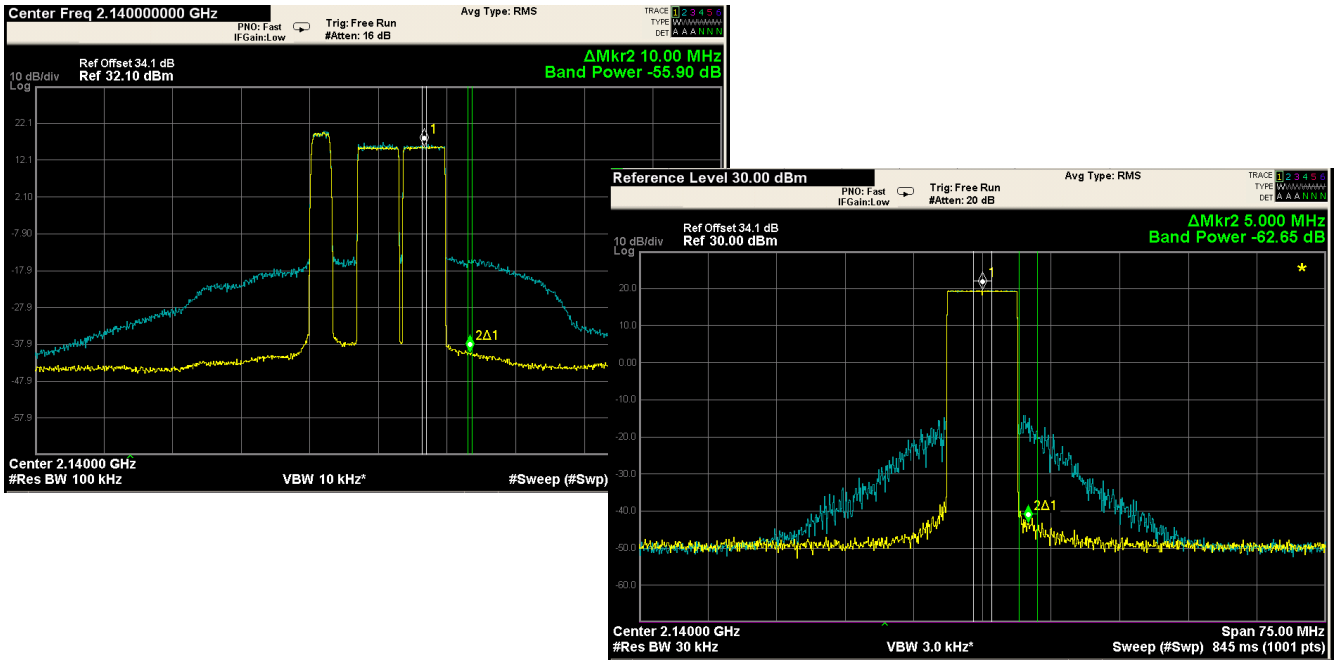

Figure 2: FlexDPD illustrative performance.

[1] Which could be another embedded processor.

Support

Systems4Silicon's FlexDPD is supplied with a comprehensive engineering data sheet and integration support tools. To facilitate system integration there is a visualisation and analysis tool which provides graphical performance and behavioural metrics for the linearized transmitter system (see Figure 3). At the core of this system is a data logging facility, the file outputs of which may be analysed locally by the system integrators or delivered to Systems4Silicon thereby facilitating remote support.

Furthermore, Systems4Silicon will not simply deliver the IP and wave goodbye. The DPD component is just one technology in a linearized transmitter system and within such systems, regardless of the DPD supplier, both the radio and (more obviously) the PA itself impact on the overall attainable performance. For example, the PA should be designed with linearization in mind and the radio bandwidth must be suitable for the anticipated linearized performance. Such design decisions and trade-offs are facilitated partly by the scalability of the FlexDPD solution, however, no less important than this is the detailed engineering knowledge and dedicated support that is provided by the Systems4Silicon team to help you attain the optimum performance for your system. Without such support, a typical DPD IP "black box" can soon drag your system to the gloomy depths of unexplainable behaviour. Systems4Silicon's IP and dedicated support and knowledge transfer team will not let you sink.

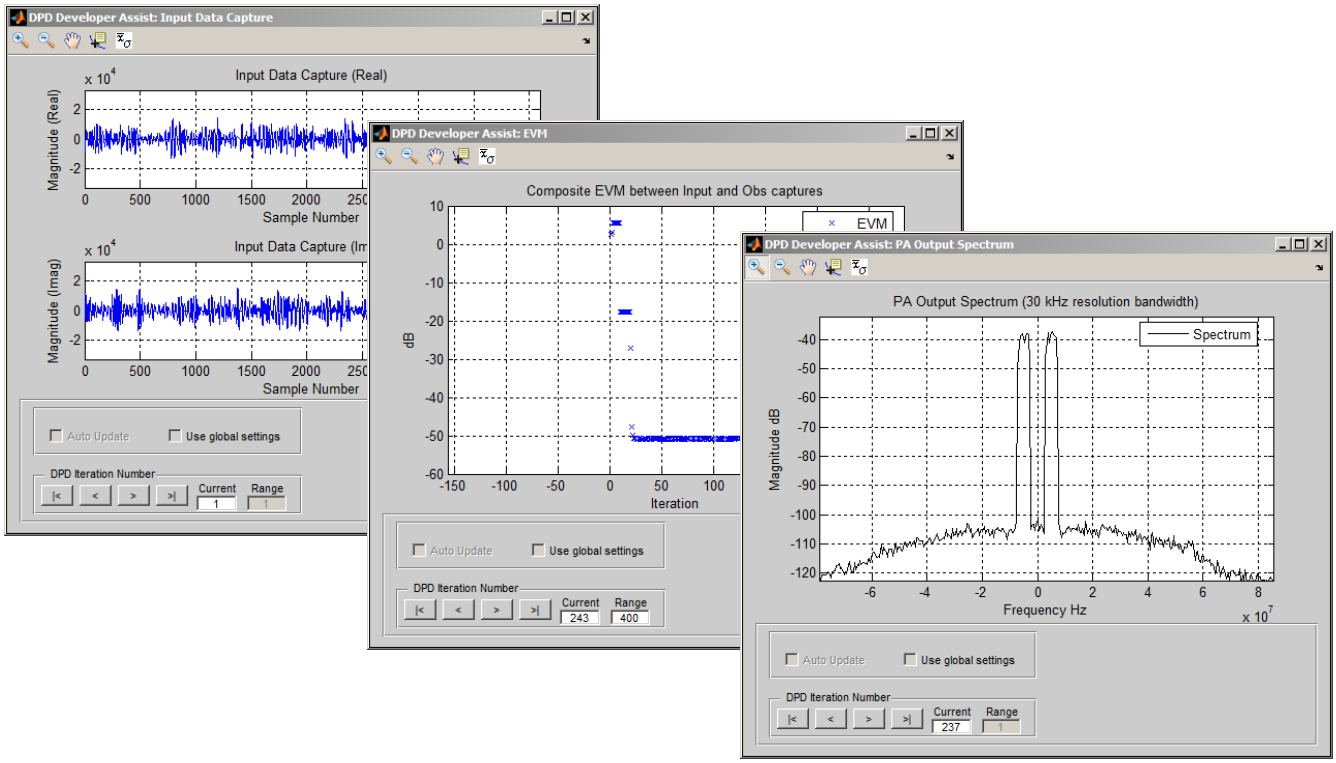

Figure 3: DPD Developer Assist integration support tool, example outputs.

Features & Capabilities

Feature	Comment
Correction capability (non-linear)	Up to 35 dB or better ACLR improvement depending upon the DPD configuration and system specifications/characteristics.
Correction capabilities (linear)	Adaptive AQM dc-offset and imbalance correction for either the transmit or observation path. Adaptive gain and phase slope correction. Adaptive gain control.
Supported transmission bandwidth	Limited only by the capabilities of the FPGA/ASIC (i.e. the attainable system clock rate) and specification of the radio sub-system. State of the art with today's FPGA and data converter devices is approximately 100 MHz of modulation bandwidth.
Supported Tx channels / MIMO	Limited only by the capabilities of the FPGA/ASIC and specification of the radio sub-system. Target technology system resources may be optimised by commutating the use of the DPD's Data Acquisition sub-system and the Adaption Processor between multiple channels. The JESD204B and gigabit transceiver capabilities of today's FPGAs combined with modern converter devices mean that device pin-out restrictions are far less likely to be a limiting factor for multiple channel support.
PA technology	Agnostic with respect to PA transistor technology or PA topology (e.g. GaS, GaN, LDMOS, Doherty, Class A/B, Envelope Tracking, …)
Transmission standards	Agnostic with respect to transmission standard (e.g. 2/3/4/5G, DVB-T, BGAN, DVB-S2X and many others) and air access technique (e.g. FDD/TDD), including multi-carrier and mixed mode operation.
DPD update cycle period	Typically, 100 ms for a single channel system. Rapid convergence algorithms result in system ACLR typically better than 1 dB of nominal minimum within 2-3 update cycles.
Memory correction	Scalable as demanded by the PA characteristics.
PA efficiency improvement	This is not a valid metric for any DPD implementation. Typically a PA will be designed to meet a particular efficiency and then the DPD enables linear behaviour at that efficiency. If, in order to meet spectral emissions, the drive to a particular PA has had to be reduced then the DPD will help to recover the original operating power level and hence efficiency. If the PA has been over-designed for the target operating power then the DPD may enable the output power and efficiency to be increased whilst maintaining linear transmission.
Convenience	In-deployment algorithmic training or calibration is not required, either at power-up or subsequently.
Crest Factor Reduction (CFR)	Crest Factor Reduction (CFR) and DPD are different yet complimentary technologies that both facilitate the enhancement of PA efficiency. Although often used together for optimum efficiency, this is a system design decision and not mandatory. Systems4Silicon's DPD operates with or without a preceding CFR function.

Target Device Resources

In addition to FlexDPD being scalable according to the application, the implementation is already extremely compact. Table 1 illustrates the resource utilisation for a typical implementation on Intel Arria 10 of a single channel system that includes comprehensive memory correction capabilities necessary for broadband operation. Should the embedded Cortex MPCore or an external processor be available then it can be seen that the demands upon the device fabric become very small indeed.

Table 1: FlexDPD resource utilisation for Intel Arria 10 part number 10AX048

	ALUTs	Dedicated logic registers	DSP block multipliers	Block Memory Kbits
DPD Adaption (Nios II/f)	8,000	8,250	13	230
DPD Core and Data Acquisition	2,800	4,850	46	224
Total	**10,800**	**13,100**	**59**	**454**
Utilisation using Nios II/f	**< 5.9%**	**< 1.8%**	**< 2.2%**	**< 1.4%**
Utilisation using Cortex MPCore or an external processor	**< 1.6%**	**< 0.7%**	**< 1.7%**	**< 0.7%**

Availability

Systems4Silicon's FlexDPD IP is immediately available for FPGA and ASIC targets together with a User Data Sheet and integration support tools. To discuss your specific implementation requirements please contact Systems4Silicon (details below).

Contact

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